

Mask Programmable CMOS Transistor Arrays for Wideband RF Integrated Circuits

Laleh Rabieirad, *Member, IEEE*, Edgar J. Martinez, and Saeed Mohammadi, *Senior Member, IEEE*

Abstract—A mask programmable technology to implement RF and microwave integrated circuits using an array of standard 90-nm CMOS transistors is presented. Using this technology, three wideband amplifiers with more than 15-dB forward transmission gain operating in different frequency bands inside a 4–22-GHz range are implemented. The amplifiers achieve high gain-bandwidth products (79–96 GHz) despite their standard multistage designs. These amplifiers are based on an identical transistor array interconnected with application specific coplanar waveguide (CPW) transmission lines and on-chip capacitors and resistors. CPW lines are implemented using a one-metal-layer post-processing technology over a thick Parylene-N (15 μm) dielectric layer that enables very low loss lines (~ 0.6 dB/mm at 20 GHz) and high-performance CMOS amplifiers. The proposed integration approach has the potential for implementing cost-efficient and high-performance RF and microwave circuits with a short turnaround time.

Index Terms—Amplifiers, coplanar waveguide (CPW), gain-bandwidth product, mask programmable technology, Parylene-N, Si CMOS, transmission line, wideband circuits.

I. INTRODUCTION

THE GROWING markets of wireless communication systems and automotive radars have stimulated the need for competitive high-performance and cost-efficient RF and microwave systems that require shorter time to develop. Both SiGe bipolar and CMOS transistors have been utilized for low-cost RF and microwave circuit realizations [1]–[3]. These circuits are typically implemented on a low-resistivity Si substrate using processes optimized for digital circuit applications. On the other hand, RF and microwave circuit design requires custom-made metallization for inductors, interconnects, and transmission lines on the lossy Si substrate. The substrate loss not only introduces signal attenuation and noise degradation through these passive elements and interconnects, but also results in distributed parasitic components and undesired

signal couplings, which are difficult to model. Therefore, the performance of the RF or microwave circuit strongly depends on the designer's experience, careful parasitic consideration, line-to-line spacing, capacitive and substrate couplings, frequency of operation, and the choice of the substrate. Clearly these factors translate into high final cost due to the intellectual proprietary and a long turnaround time (TAT). On the other hand, if the RF interconnect process, which generally does not require submicrometer features, is separated from the deep-submicrometer RF CMOS device and digital integrated circuit processes through a post-fabrication technology, the digital CMOS platform can be easily mask programmed to implement different RF functions without a need to customize the Si chip for each application.

In this paper, for the first time, we report a mask programmable post-fabrication integration technology applied to high-performance CMOS transistor arrays for RF and microwave applications. The integration is performed through definition of RF interconnect patterns on an array of 90-nm RF CMOS transistors coated with a thick (15 μm) Parylene-N dielectric layer. Parylene-N has very low loss and low dielectric constant characteristics, which result in high-performance passive components and interconnects [4] without a need for shield ground levels [8]. By developing low-loss coplanar waveguide (CPW) transmission lines on Parylene-N in this post-fabrication technology, three wideband RF amplifiers based on an identical transistor array, but different RF interconnects are implemented. These amplifiers show high transmission gain of above 15 dB and large gain bandwidth products of above 79 GHz. Although this work is focused on RF performance of transmission lines and their realization in RF wideband amplifiers rather than the achievable miniaturization, RF circuits with smaller chip sizes can actually be obtained in this technology through using bent transmission lines and array chips with shorter distances between the array cells.

The proposed mask programmable technology can be used to implement high-performance RF and microwave functions in a short TAT and at a very low cost. The low loss and low parasitic characteristics of passive components and interconnects on the thick Parylene-N dielectric material result in high-performance and easy-to-model RF and microwave components and circuits on the lossy Si substrate. In Section II, a background on various techniques to implement configurable RF designs is provided. In Section III, details of the mask programmable technology performed on CMOS transistor arrays is described. Transmission line optimization and wideband amplifier circuit design are discussed in Section IV. In Section V, measurement results of various wideband amplifiers fabricated in this work are discussed. In Section VI, the performance and application

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L. Rabieirad was with the School of Electrical and Computer Engineering and the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA. She is now with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: laleh@caltech.edu).

E. J. Martinez is with the RF Technologies Division, Raytheon Network Centric Systems, Fort Wayne, IN 46808 USA (e-mail: Edgar.J.Martinez@raytheon.com).

S. Mohammadi is with the School of Electrical and Computer Engineering and the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: saeedm@purdue.edu).

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of this technology is discussed, while a brief summary of the study is provided in Section VII.

II. BACKGROUND

Configurable and reconfigurable analog and RF circuits have been proposed for multistandard communication systems [5]–[10]. Software programming of multifunctional hardware, while being reconfigurable in real time, does not yield optimum performance for a specific application [5]–[7]. Tradeoffs and challenges involved are high power consumption due to wideband low-noise amplifiers (LNAs), full-band digitization requirements, and the need to implement a wide tuning range local oscillator (LO) [5], need for different RF branches [6], or need for multiple switchable bandpass filters with a radio architecture susceptible to nonlinearities [7]. On the other hand, in [8] and [9], a method is proposed to integrate GaAs MESFETs or Si bipolar transistors using several layers of Au metallization and polyimide and obtain configurable circuits through two-step processing. First, devices and a lower metallization layer of metal–insulator–metal (MIM) capacitors are implemented to form master-slice arrays. A stack of metallization layers separated by thin polyimide layers are then deposited on top of the device layer to construct passive components and interconnects and achieve configurable circuit functions. While this method uses a complex multilayer fabrication on high-cost GaAs or Si bipolar devices, its important advantages are to reduce the TAT by almost a factor of 2 and the overall cost by 50%–75% assuming that GaAs or Si bipolar device layers are prefabricated at high volume.

Mask configurable narrowband RF LNAs and RF receivers have been studied in [10]. An SiGe BiCMOS process is utilized to design various RF circuits using an identical transistor footprint. Only upper metal and via layers are altered in the process to achieve RF front-ends for global positioning system (GPS), wideband code division multiple access (W-CDMA), and wireless local area network (WLAN) applications. The upper metal layer is still part of the back-end-of-line (BEOL) process. Therefore, not only is the performance limited by the passive components on a standard BiCMOS process, but there is also no reduction in the TAT for the three individual designs.

III. TECHNOLOGY

A. Technology Overview

Current RF integrated circuits (RFICs) and monolithic microwave integrated circuits (MMICs) are incorporated based on integrating passive and active components on a single Si or compound semiconductor technology platform. These platforms use deep-submicrometer processes to realize high-performance active devices that are relatively small in size compared to the overall size of the RF or microwave chip. The remaining chip is devoted to large passive components such as inductors and transmission lines or is not utilized for various electromagnetic and layout considerations. In the case of Si-based RFICs and MMICs, capacitive couplings combined with the losses induced by the low-resistivity Si substrate result in low quality factor

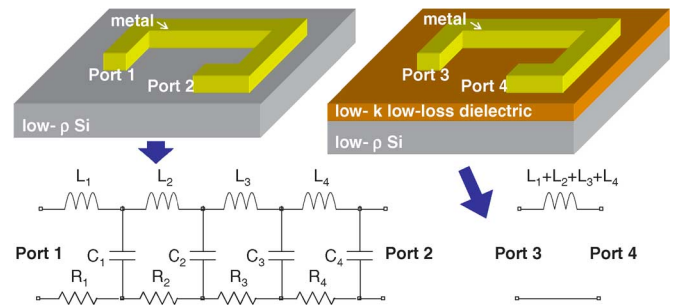


Fig. 1. (left) Inductor and interconnect lines implemented directly on Si substrate are lossy and have complicated equivalent-circuit models. (right) By adding a thick low- k low-loss dielectric layer below the metal interconnect line or inductor, distributed parasitic capacitive terms in the device model are suppressed. Therefore, the lossy Si substrate is no longer the common ground plane, as coplanar mode rather than microstrip mode is dominant, resulting in a more ideal device model.

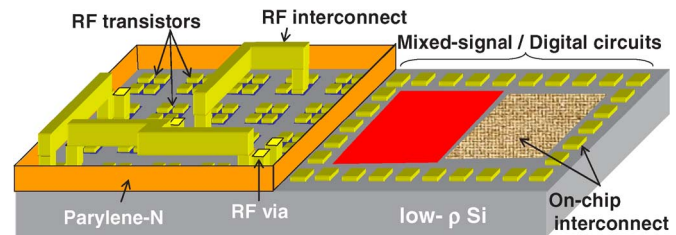


Fig. 2. Mask programmable RF system realized on a standard digital/mixed-signal Si process through a post-fabrication technology.

passives, significant RF power dissipation in the passive network, crosstalk, thermal noise injection, and added difficulties in component modeling and circuit simulation.

As shown in Fig. 1, if a passive component such as an inductor, transmission line, or RF interconnect is elevated from the lossy Si substrate by a thick low-loss and low-permittivity dielectric layer, the dielectric loss, and hence, the signal attenuation through the component, is reduced. The CPW mode rather than the microstrip mode can become dominant in the component through a cautious design in which the shortest path from any point on the component to the ground plane is not through the lossy substrate. Therefore, the equivalent-circuit model for the component reduces to a more ideal interconnect, transmission line, or inductor shown in Fig. 1, as distributed parasitic capacitance between the component and the lossy substrate is significantly reduced. The low-loss low-permittivity dielectric material used in this work is Parylene-N with a measured permittivity of 2.35–2.4 and a loss tangent of less than 6×10^{-4} up to 60 GHz [4].

B. Array Design

Fig. 2 envisions a mask programmable RF system. On this system, mixed-signal and digital signal processing circuits and an array of RF transistors are first fabricated in a standard CMOS or BiCMOS technology. In our study, a standard 90-nm CMOS technology is used to implement a 4×5 array of RF transistors and passive components, as shown in Fig. 3. In order to provide versatility for a wide range of RF applications, the footprint of the array is designed with various transistor cells,

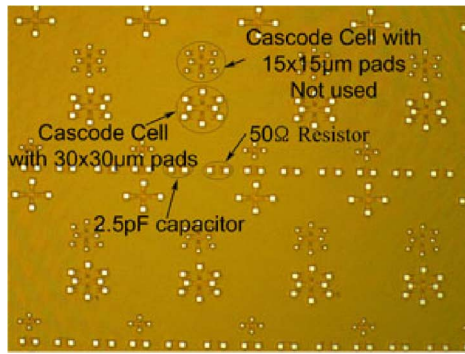


Fig. 3. Microphotograph of part of the 4×5 array of a CMOS chip with chip dimensions of $4 \text{ mm} \times 4.8 \text{ mm}$. Typical devices used in this work are shown.

TABLE I
DIELECTRIC PROPERTIES OF SEVERAL THIN-FILM MATERIALS

Property	Parylene-N	Silicon Dioxide	Polyimide	SU-8
Dielectric Constant (ϵ)	2.4	3.9	3.4	3.6
Loss Tangent $\tan(\sigma)$	6×10^{-4}	2×10^{-5}	0.001	0.037
Volume Resistivity ($\Omega\text{-cm}$)	1.4×10^{17}	$>10^{18}$	1.5×10^{17}	3×10^6
Melting Point ($^{\circ}\text{C}$)	420	>1500	520	82

resistors, and capacitors. Devices that are utilized in this study are multifinger cascode transistor pairs with dimensions of $W/L = 150 \text{ } \mu\text{m}/90 \text{ nm}$, 2.5-pF capacitors for ac coupling, and 50- Ω resistors. These devices are connected to contact pads with dimensions of $30 \text{ } \mu\text{m} \times 30 \text{ } \mu\text{m}$ with a parasitic capacitance to the substrate of 12 fF verified by measurement and deembedding of devices with and without pads. The parasitic capacitance of each pad introduces additional current drive requirement ($\Delta I = C_{\text{parasitic}} \cdot j\omega \cdot \Delta V$). Smaller pad dimensions not utilized in this study result in smaller capacitance and smaller current drive requirement. The capacitance can also be absorbed as part of a matching network or through adjusting the dimensions of the transmission line ending connected to the pad [11], [12].

C. Post-Fabrication

In the post-processing fabrication, a 15- μm -thick conformal Parylene-N layer is first deposited on top of the CMOS transistor array at room temperature using the process described in [4]. Parylene-N is selected for its simple fabrication at room temperature, its low dielectric constant, and extremely low dissipation factor (loss tangent). Parameters of Parylene-N and a few other materials are compared in Table I. Unlike silicon dioxide, Polyimide, and other high-temperature passivation layers, the deposition of Parylene-N is done at room temperature, making it suitable for coating devices and circuits with limited thermal

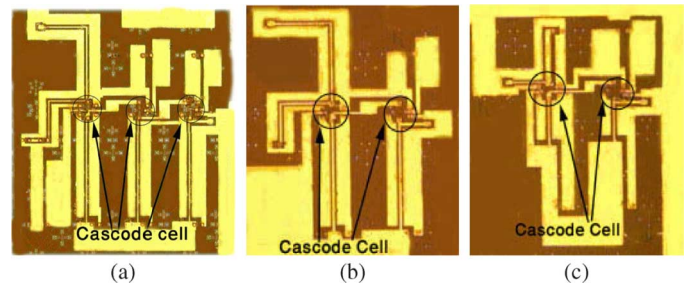


Fig. 4. Micrographs of final chips. (a) Amp1, area: $3 \text{ mm} \times 3.4 \text{ mm}$. (b) Amp2, area: $2.15 \text{ mm} \times 3.4 \text{ mm}$. (c) Amp3, area: $2 \text{ mm} \times 3.4 \text{ mm}$.

budget. The drawback of Parylene-N is its large thermal mismatch to Si (69 ppm/C compared to 3.2 ppm/C for Si [4]), which prohibits its application for large-area electronics that are subjected to high temperature variations. The thickness of Parylene-N in this study is adjusted to 15 μm in order to achieve a thick enough dielectric layer to significantly reduce loss and parasitic coupling to the Si substrate while keeping the vias through the dielectric layer relatively short to achieve good microwave performance and high manufacturing yield. In the following steps of the process, lithography and reactive ion etching (RIE) (plasma O_2 with 990 sccm flow rate for 45 min) are used to create via-holes in the Parylene-N layer to access the pads of the cells that are used in a specific design [13]. Next, RF interconnect metallization lines are defined using lithography, sputtering, and liftoff of Ti (0.05 μm) and Au (0.3 μm). The walls of vias are covered with metal through the sputtering process to ensure good dc contacts. To improve the RF contact of vias and reduce the metal loss of RF interconnect lines, Au electroplating is performed to increase the thickness of RF interconnect lines to 3 μm .

By altering via and metallization masks (so-called mask programming), three different wideband amplifiers are fabricated on identical array chips using the above post-fabrication technology. Fig. 4(a)–(c) shows microphotograph images of the fabricated amplifiers. Amplifier 1 (Amp1) occupies $3 \text{ mm} \times 3.4 \text{ mm}$ of the chip area, while amplifier 2 (Amp2) and 3 (Amp3) occupy areas of $2.1 \text{ mm} \times 3.4 \text{ mm}$ and $2 \text{ mm} \times 3.4 \text{ mm}$, respectively.

IV. CIRCUIT DESIGN

A. CPW Transmission Lines

In this work, CPW transmission lines are used to design wideband amplifiers. Thick Parylene-N layer underneath the CPW lines significantly reduces the RF signal loss by diminishing eddy currents in the low-resistivity Si substrate. A low dielectric constant of Parylene-N lowers the line capacitance per length and thus increases the characteristic impedance of the CPW transmission line. Due to the thick dielectric layer, the microstrip mode weakens and the quasi-TEM mode becomes the dominant mode in the CPW line [14], [15]. The characteristic impedance of such low-loss CPW lines is independent of the dielectric layer thickness (and its variations) and is set by two parameters, center conductor width W , and the distance between the center conductor and the ground planes G . Both W

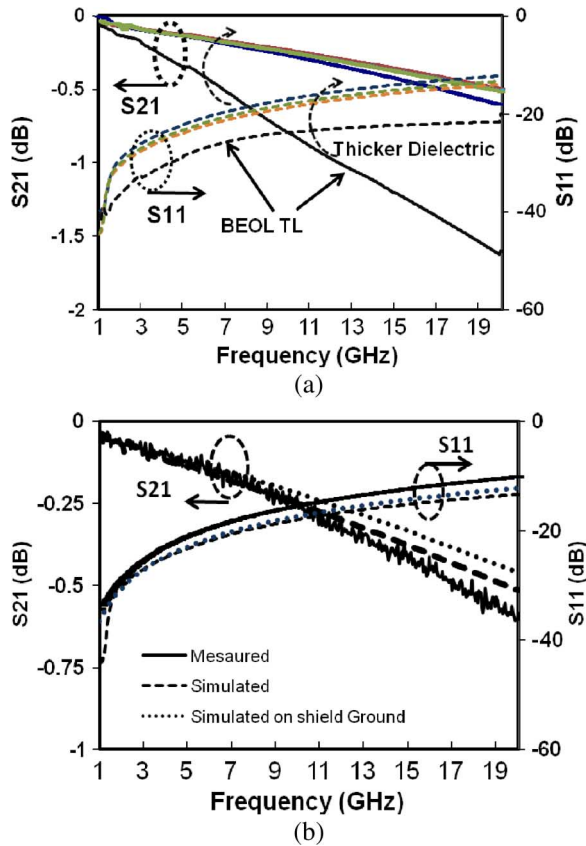


Fig. 5. (a) Simulated loss of a 1-mm CPW line for different Parylene-N thicknesses (CPW line dimensions: $W = 21 \mu\text{m}$, $G = 28 \mu\text{m}$). CPW line is on top of $1 \Omega \cdot \text{cm}$ resistivity Si substrate and a $5\text{-}\mu\text{m}$ -thick silicon dioxide, all part of the BEOL technology. For all lines, except the BEOL CPW line, there is also a $5\text{-}\mu\text{m}$ BEOL polyimide layer and an extra 10-, 12-, and $15\text{-}\mu\text{m}$ Parylene-N underneath the line as a result of the proposed post fabrication integration technology. (b) Comparison between the simulation and measurement of the S -parameters of CPW line on $15\text{-}\mu\text{m}$ Parylene-N ($W = 21 \mu\text{m}$, $G = 28 \mu\text{m}$, $L = 1 \text{ mm}$) along with the simulation result of the same CPW line with an additional ground plane between the substrate and silicon-dioxide layer.

and G can be easily changed by modifying only the top metal layer. This characteristic makes the CPW line an appropriate choice for the integration technology.

Ansoft Technologies' High Frequency Structure Simulator (HFSS) is used to design the CPW lines on the CMOS substrate (CMOS BEOL process: $1.3\text{-}\mu\text{m}$ Al metal layer on a $5\text{-}\mu\text{m}$ -thick SiO_2 and covered with $5\text{-}\mu\text{m}$ Polyimide passivation layer) and on Parylene-N layer. Fig. 5(a) shows the simulated S -parameters of a 1-mm CPW line for the BEOL process, as well as the ones on different thicknesses of Parylene-N. This figure suggests that the loss of the line with $10 \mu\text{m}$ or thicker Parylene-N is significantly lower than the BEOL line. By using $15\text{-}\mu\text{m}$ -thick Parylene-N compared to the BEOL line, the transmission loss of the CPW line is reduced by 1.1 dB/mm to $\sim 0.5 \text{ dB/mm}$ at 20 GHz . The difference in loss of CPW lines with $W = 21 \mu\text{m}$, $G = 28 \mu\text{m}$ and with Parylene-N thicknesses of $10\text{--}15 \mu\text{m}$ is also insignificant, pointing to the elimination of the Si substrate loss at such thicknesses. The small difference also suggests that the RF performance of transmission lines is independent of the variations in the thickness of the dielectric layer. For small via openings, a Parylene-N dielectric layer thicker than $15 \mu\text{m}$ may

pose fabrication difficulties due to high aspect ratio vias. Additionally, parasitic inductance due to long via length may be of concern at microwave and millimeter-wave frequencies. HFSS simulation shows that a $15\text{-}\mu\text{m}$ via length creates a 14-pH inductance for a $30 \mu\text{m} \times 30 \mu\text{m}$ pad dimensions. Therefore, CPW lines with the above dimensions of $W = 21 \mu\text{m}$, $G = 28 \mu\text{m}$ on $15\text{-}\mu\text{m}$ thick Parylene-N are used for the circuit design. These lines show a characteristic impedance of 70Ω .

To verify the accuracy of the simulation, we have fabricated CPW lines with $W = 21 \mu\text{m}$, $G = 28 \mu\text{m}$ and on a $15\text{-}\mu\text{m}$ Parylene-N dielectric layer coating a typical CMOS substrate. Fig. 5(b) shows a good agreement between measured and simulated S -parameters. In order to obtain the inherent S -parameters of the fabricated CPW lines, an open-thru deembedding technique on measured S -parameters is performed [16]. The measured loss of fabricated CPW lines is 0.6 dB/mm at 20 GHz .

Si and SiGe RF and microwave integrated circuits often use shielded microstrip-mode CPW lines and shielded inductors to provide isolation of these components from the Si substrate in which the underlying ground plane prevents the electromagnetic field from penetrating the lossy substrate [17]–[20]. In order to investigate if shielding can provide additional substrate isolation in this mask programmable technology, we have performed HFSS simulation of S -parameters of a CPW line with a ground plane underneath, as shown in Fig. 5(b). The results indicate that additional shielding does not provide significant improvement over the CPW line without the shielded line. This emphasizes the fact that a $15\text{-}\mu\text{m}$ Parylene-N layer is thick enough to isolate the CPW line from the substrate and crosstalks.

B. Wideband Amplifiers

Three multistage wideband amplifiers with cascode transistor pairs with W/L of $150\text{-}\mu\text{m}/90\text{-nm}$ and $70\text{-}\Omega$ CPW transmission lines on Parylene-N are designed. Cascode gain stage is superior to the common-source transistor in terms of overall circuit RF gain, bandwidth, stability, and input to output isolation. Fig. 6 shows the schematic of the three-stage (Amp1) and two-stage (Amp2 and Amp3) amplifiers designed in this work. Capacitors (2.5 pF) and resistors (50Ω) from the prefabricated array are utilized to provide matching and coupling for the input port, as well as bypassing the dc bias ports, as shown in Fig. 6. Since no RF model is provided in this digital CMOS technology, S -parameters of cascode pair transistors including their RF pads are measured under various bias conditions. Open-thru deembedding on measured data is performed to extract the S -parameters of the cascode cell without the connecting RF pads [16]. Various sections of transmission lines including their bends are simulated separately using HFSS. Simulated S -parameters of different transmission line sections are combined with the measured (and deembedded) S -parameters of the cascode cells in a circuit simulator environment (Ansoft Designer).

V. CIRCUIT CHARACTERIZATIONS AND DISCUSSIONS

Two-port S -parameter measurements of the fabricated amplifiers are performed using the Agilent 8722 network analyzer and on-wafer probing. Calibration is done using a short-open-load-thru (SOLT) standard substrate. S -parameters of all three amplifiers are shown along with the simulation results in Fig. 7.

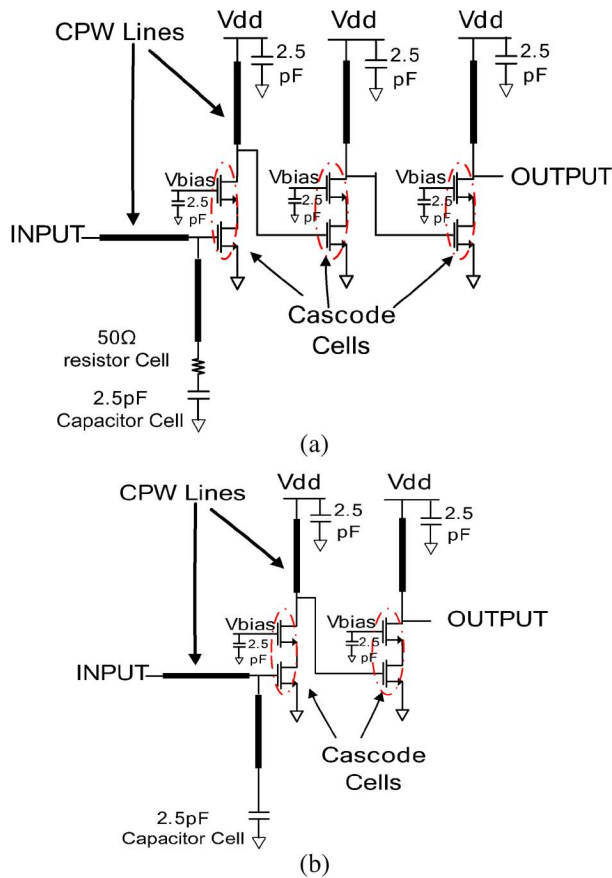


Fig. 6. Schematics of: (a) three-stage (Amp1) and (b) two-stage amplifiers (Amp2 and Amp3). Transistor dimensions: $W = 150 \mu\text{m}$, $L = 90 \text{ nm}$, number of fingers = 100.

As shown, Amp1, shown in Fig. 4(a) with three cascode stages, has a high S_{21} gain of 19 dB and a bandwidth of 3.9–14.8 GHz with an overall gain-bandwidth product of 96.7 GHz. The dc power dissipation of this amplifier is only 57.6 mW. Amp2, shown in Fig. 4(b), uses two cascode stages and achieves an S_{21} gain of 17.6 dB over a bandwidth of 5.4–16 GHz and an overall gain-bandwidth product of 80 GHz. Its power dissipation despite having only two stages is higher than Amp1 at 80.3 mW. Amp3, shown in Fig. 4(c), is another two-stage cascode amplifier with slightly shorter transmission lines compared to those of Amp2. It achieves a S_{21} gain of 15 dB over a bandwidth of 7.8–22 GHz. The overall gain-bandwidth product of this amplifier is still high at 79 GHz with a power dissipation of 62.7 mW. There are some discrepancies in the simulated and measured S -parameter response of these amplifiers. These discrepancies are attributed partially to the errors in deembedding the measured transistor cells and partially the effect of connecting the S -parameter boxes without considering the effect of possible interaction between them.

As it is shown here, when the designs of top metallization and vias in the simple post-fabrication technology are altered while using the same active cells, a variety of circuit applications and bandwidth requirements are achieved. The mask programmability is achieved by changing the schematic of the circuits for various applications and by adjusting the value of passive components in each schematic, i.e., the schematic of Amp1 is different from the other two amplifiers, while Amp2 and Amp3 are

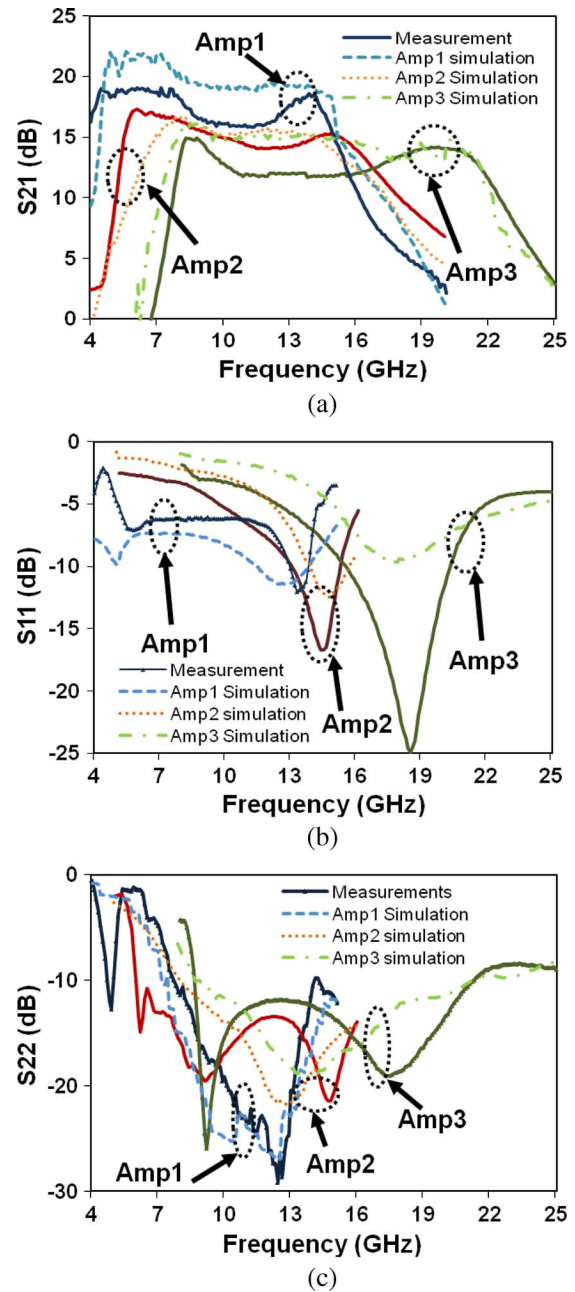


Fig. 7. Measurement and simulation results of S -parameters for the three wideband amplifiers fabricated in this study. (a) S_{21} . (b) S_{11} . (c) S_{22} .

based on the same schematic having different frequency bands. By using up to 71% shorter CPW lines in Amp3 compared to Amp2, the higher 3-dB frequency has been increased from 15 to 22 GHz, showing the capability of this technology for circuits in higher frequencies.

VI. DISCUSSION

Cascaded wideband amplifiers have been used to provide high-gain amplifiers [27]. In the amplifiers implemented here, a gain per stage of 6.3–8.8 dB are achieved. While Mitomo *et al.* have reported higher gain per stage values at 60 GHz [18] than those achieved here, their implementation is based on a smaller bandwidth of operation. Table II compares the results obtained from this work with the state-of-the-art high

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Ref	S_{21} (dB)	BW (GHz)	# of stages	Cell type	Gain \times BW (GHz)	P_{diss} (mW)	Technology
[1]	14	0-73.5	3	DA	370	84	CPW 90nm CMOS
[17]	19.7	48-55.8	3	CC	75	75	90nm CMOS
[21]	9.5	0-32	5	CC	95	99	0.18 μ m CMOS
[22]	5	0-40	4	CS	71.1	24	0.13 μ m CMOS
[23]	8.8	0-29.5	5	CC	81.2	480	0.13 μ m BiCMOS
[24]	9.8	0-44	8	CC	136	103	0.13 μ m CMOS
[25]	7.4	0-80	6	CC	187.5	120	90nm CMOS
[26]	18	58-65	1	Diff-CC	55.6	240	SiGe BiCMOS
[19]	23.8	74-80	2	Diff-CC	93	61.25	SiGe BiCMOS
[27]	15	0-28	2	CC	157	48	SiGe BiCMOS
This work - Amp 1	19	3.9-14.8	3	CC	96.7	57.6	CPW 90nm CMOS
This work - Amp 2	17.6	5.4-16	2	CC	80	80.3	CPW 90nm CMOS
This work - Amp 3	15.0	7.8-22	2	CC	79	62.7	CPW 90nm CMOS

Cell types: CC: cascode. CS: common source. DA: distributed amplifier

gain-bandwidth product amplifiers that are designed in various Si CMOS and SiGe BiCMOS processes (see [1] and [17] and [19]–[27]). Note that these distributed amplifiers are optimized based on transistor size, number of stages, and transmission line dimensions to achieve the largest possible bandwidths or gain-bandwidth products. The multistage wideband amplifiers reported in this work are not based on the distributed amplifier topology; nevertheless, they achieve very high bandwidth and gain-bandwidth products at relatively low power dissipation. The three CMOS distributed amplifiers with higher gain-bandwidth products than those achieved in this work either use 6–8 stages of amplifications (see [24] and [25]) or use a feedback in the amplification path and additional distributed amplifiers for input and output matching [1]. Additionally, SiGe wideband amplifiers using transistors with cutoff frequencies above 200 GHz has been used in [19] and [27] in order to achieve the high gain-bandwidth products.

While this work is mainly based on the study of transmission lines, optimization of the fabrication technology, and the application of the mask programmable technology in high gain-bandwidth product amplifiers, the miniaturization of circuits is not emphasized, resulting in rather large chip sizes for each circuit. Transmission lines implemented in the amplifiers are straight lines causing a large area allocated to each circuit. Implementing bent lines in this technology can be easily achieved due to the conformal coverage of thick Parylene-N, as shown in Fig. 8(a). Simulation confirms that large thickness of the Parylene-N layer eliminates the effect of the unused components underneath the line, resulting in more compact circuits that can be directly implemented over the active components and their large pads. Additionally, S -parameter measurement of both bent and straight lines with identical signal width, signal to ground gap, and length show that bending the line without using ground equalizing air-bridges would increase the loss of the line by only 0.24 dB/mm at 20 GHz, as shown in Fig. 8(b). Implementing

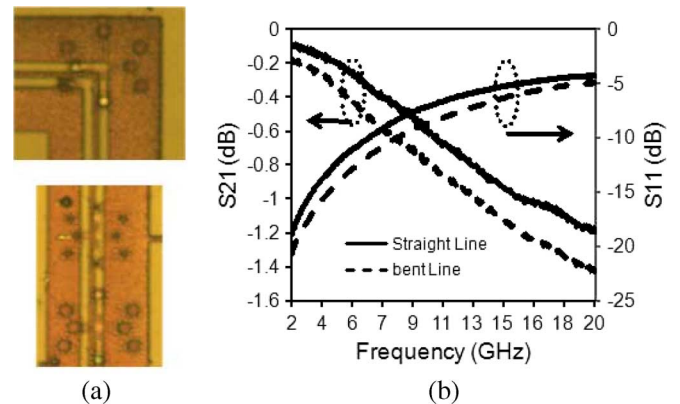


Fig. 8. (a) Micrograph pictures of straight and bent transmission lines over unused active cells. (b) Measured S -parameter of a straight and bent CPW lines with $W = 12.5 \mu\text{m}$, $G = 40 \mu\text{m}$, and $L = 1 \text{ mm}$.

pre-fabricated underpasses for ground equalization would remove the extra loss of the bent structure and facilitate more compact chip areas without further complicating the post-processing fabrication.

While advanced CMOS and BiCMOS processes have several deep submicrometer metallization with $<50\text{-nm}$ alignments, which requires planarization, using deep UV light sources and special masks, the proposed RF mask programmable technology only requires one interconnect metallization path with a width of at least several micrometers. Therefore, the minimum feature size for RF interconnects, inductors, and transmission lines on the top level can be easily set to $1 \mu\text{m}$ without any performance loss. As the integration technology relies on a simple one-step metallization and $1\text{-}\mu\text{m}$ feature optical lithography on a fixed array chip, the fabrication time for each new circuit is reduced to a few days rather than the few weeks needed for metal processes of a standard CMOS process. The wideband

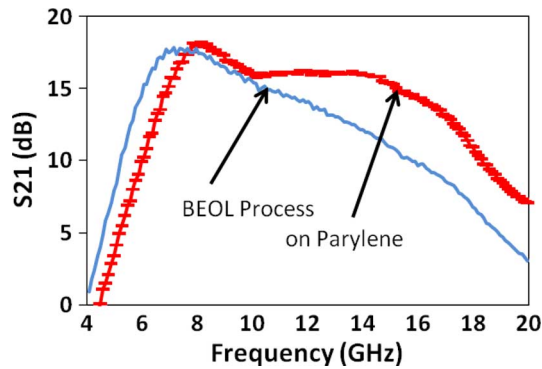


Fig. 9. Simulated forward transmission coefficients S_{21} of AMP2 with and without Parylene-N layer using identical transistors and similar power dissipation, but optimized transistor biasing and transmission line sections.

amplifier circuits reported here are fabricated in a very short TAT and achieve very good performance with only two or three cascaded stages. This clearly demonstrates the capability and versatility of the proposed mask-programmable technology.

Material cost constitutes the majority of the integration and packaging cost [28], [29]. In the post-processing integration, one layer of Parylene-N, one electroplating step, and two mask alignments are used. The alignments in this technology do not require submicrometer precision and expensive deep submicrometer masks. Parylene-N deposition is done at room temperature in a batch process in which many parts can be coated at the same time. These features make the post fabrication technology very cost efficient and simple. Combined with good RF circuit performance, short TAT, and the ability to configure to any RF and microwave circuit requirement, the low-cost post-fabrication technology described here would be a very suitable choice for RF and microwave system implementation. The only limitation of the technology is that the sizes and relative distances of RF transistors and resistors and capacitors are predefined and cannot be varied. To alleviate this limitation, various transistors, gain cells, and lumped passive components are implemented in each array element. Additionally, for lower RF frequencies, neighboring transistor cells can be effectively combined into one cell to achieve higher transconductance and current drive capability. Therefore, the proposed mask programmable technology is useful in applications in which low-cost RF circuits with short TAT are required.

To demonstrate the importance of a thick low-loss dielectric layer (in this work, Parylene-N) and thick interconnect metallization ($3\text{ }\mu\text{m Au}$) in achieving good RF performance, we have compared simulation results of Amp2 (with a total bias current of 73 mA) with an optimized two-stage BEOL amplifier without a Parylene-N layer. Simulation of the new two-stage circuit is performed using the same cascode transistor sizes ($150\text{ }\mu\text{m}/90\text{ nm}$) biased under a slightly different optimum total current of 75 mA and slightly different dimensions of CPW lines (typically 13%–23% shorter compared to Amp2 due to a higher effective dielectric constant on Si). The CPW lines in the BEOL process use $1.3\text{ }\mu\text{m}$ of Al metallization and are placed on a $5\text{-}\mu\text{m}$ -thick silicon-dioxide layer and Si substrate with $1\text{ }\Omega\cdot\text{cm}$ resistivity. In the mask programmable design of Amp2, CPW

lines are on top of an additional $5\text{-}\mu\text{m}$ BEOL polyimide passivation layer and a $15\text{-}\mu\text{m}$ -thick Parylene-N layer. Fig. 9 compares the results for S_{21} gain obtained for these two optimum cases. As this figure suggests, with almost the same power dissipation (80.3 and 82.5 mW), gain at high frequencies ($f > 9\text{ GHz}$) and bandwidth of Amp2 is much higher than the one achieved using standard CMOS technology directly on the CMOS substrate (BW of 10.6 GHz for Amp2 compared to 4.95 GHz for BEOL design). The difference is mainly due to significant reduction of substrate coupling and loss at higher frequencies through using the $15\text{-}\mu\text{m}$ Parylene-N layer and $5\text{ }\mu\text{m}$ BEOL polyimide underneath the CPW lines.

VII. CONCLUSION

A new mask programmable integration technology based on an array of 90-nm transistors and a low-loss low-permittivity dielectric material (Parylene-N) is introduced. The technology involves a one-layer passivation and metallization. Programmability (RF circuit configuration) is achieved through patterning vias and the top metal layer. The effect of Parylene-N as a passivation layer on the insertion and return loss of CPW lines is studied. It is found that a $15\text{-}\mu\text{m}$ -thick Parylene-N layer is suitable for typical dimensions of $70\text{-}\Omega$ CPW lines used in this study ($W = 21\text{ }\mu\text{m}$ and $G = 28\text{ }\mu\text{m}$). Three wideband amplifiers operating up to 22 GHz with different bandwidths from 10.6 to 14.2 GHz are fabricated. These amplifiers based on CMOS 90-nm cascode transistor pairs and low-loss CPW lines on top of the $15\text{-}\mu\text{m}$ Parylene-N layer provide high forward transmission gains above 15 dB.

They achieve high gain-bandwidth products in the range of 79–96 GHz and compare well with the state-of-the-art CMOS distributed amplifiers in spite of using standard multistage topologies. This technology not only provides better high-frequency performance compared to similar circuits in standard CMOS technology, but it also provides the option of programmability. In addition, the simple fabrication process and design procedure makes this technology desirable for low cost and short time to market RF and microwave circuits and systems. The wideband amplifiers introduced here are optimized based on exploring the capability of this technology in providing high gain-bandwidth product rather than very high operating frequencies. More research needs to be conducted in order to study the potentials of mask programmable technology for very high frequencies in comparison to the amplifiers already achieved in Si and SiGe technologies [1], [19], [25], [26].

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Laleh Rabieirad (S'04–M'09) received the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, in 2008.

She is currently a Postdoctoral Fellow with the California Institute of Technology, Pasadena. During the summer and fall of 2006, she was a Student Intern with Freescale Semiconductors Inc., Tempe, AZ. Her research interests are microwave and RF reconfigurable circuits and integrated circuit design.



Edgar J. Martinez received the Ph.D. degree in electrical engineering from the University of Virginia, Charlottesville, in 1995.

He is currently the Manager of the RF Technologies Division, Raytheon Network Centric Systems, Fort Wayne, IN. From 2007 to 2008, he was the Associate Dean for Interdisciplinary Programs with the College of Engineering, University of Illinois at Urbana-Champaign. From 2004 to 2007, he was the Assistant Dean of Engineering for Research and Entrepreneurship with Purdue University. He was a Program Manager with the Microsystems Technology Office, Defense Advanced Research Projects Agency (DARPA) until 2004, and with the Air Force Research Laboratory, Dayton, OH, until 1998. He has authored or coauthored over 100 publications and invited conference presentations.

Dr. Martinez is a member of the Electro-chemical Society and the American Society of Engineering Education.



Saeed Mohammadi (S'89–M'92–SM'02) received the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 2000.

He is currently an Associate Professor of electrical and computer engineering with Purdue University, West Lafayette, IN. His group is involved in research in RF devices and circuits, RF integration, and nanoelectronic technology. He has authored or coauthored over 100 journal and refereed conference papers in these areas.

Dr. Mohammadi was an associate editor for the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS from 2006 to 2007.